IN THE CLAIMS

Please amend the claims as follows:

Claims 1-8 (Cancelled).

Claim 9 (Currently Amended): A semiconductor device at least having a nonvolatile ~~semiconductor~~ memory at least having a memory cell array structure that comprises:

active regions extending linearly in parallel with one another and containing impurity diffused source and drain regions;

element isolation regions extending linearly and isolating the active regions from one another;

gate electrodes orthogonally crossing the active regions and element isolation regions and each having a floating gate and a control gate laid one upon another;

first conductors formed from a first metal wiring layer, the first conductors extending linearly in parallel with the gate electrodes and each connecting the source regions to one another between adjacent ones of the gate electrodes; and

second conductors formed from a second metal wiring layer that is above the first metal wiring layer, the second conductors orthogonally crossing the gate electrodes and connected to the drain regions through contacts.

Claim 10 (Currently Amended): The semiconductor device ~~nonvolatile semiconductor memory~~ of claim 9, wherein the memory cell array structure further comprises:

floating electrode isolation regions orthogonally crossing the gate electrodes and isolating the floating electrodes from one another.

Claim 11 (Currently Amended): The semiconductor device ~~nonvolatile semiconductor memory~~ of claim 9, wherein:

the element isolation regions have trenches.

Claim 12 (Currently Amended): The semiconductor device ~~nonvolatile semiconductor memory~~ of claim 9, wherein:

the memory cell array structure contains NOR memory cells.

Claim 13 (Currently Amended): The semiconductor device ~~nonvolatile semiconductor memory~~ of claim 9, wherein the memory cell array structure further comprises:

source contacts each connecting one of the source regions to a corresponding one of the first conductors; and

drain contacts each connecting one of the drain regions to a corresponding one of the second conductors,

wherein the source regions and drain regions being symmetrical with each other about the gate electrodes.

Claim 14 (Currently Amended): The semiconductor device ~~nonvolatile semiconductor memory~~ of claim 13, wherein:

the source regions and drain regions substantially have an identical impurity concentration.

Claim 15 (Currently Amended). The semiconductor device ~~nonvolatile semiconductor memory~~ of claim 13, wherein:

a bit line and the second conductors are being connected further than the first conductors in a upper layer.

Claim 16 (Currently Amended): The semiconductor device ~~nonvolatile semiconductor memory~~ of claim 9, wherein a sheet resistance value of the first conductors is 1/1000 or below of a sheet resistance value of the source regions.

Claim 17 (Currently Amended): The semiconductor device ~~nonvolatile semiconductor memory~~ of claim 9, wherein:

the first conductors ~~is~~ are made of material selected from a group consisting of aluminum and aluminum-based alloys.

Claim 18 (Currently Amended): The semiconductor device ~~nonvolatile semiconductor memory~~ of claim 9, wherein the first and second conductors are made of a copper.

Claims 19-24 (Cancelled).